EXHIBIT J

United States Patent [19]

Takemae

[11] **Patent Number: 4,692,689**

[45] **Date of Patent: Sep. 8, 1987**

[54] **FET VOLTAGE REFERENCE CIRCUIT WITH THRESHOLD VOLTAGE COMPENSATION**

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[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[21] Appl. No.: **15,529**

[22] Filed: **Feb. 12, 1987**

Related U.S. Application Data

[63] Continuation of Ser. No. 663,712, Oct. 22, 1984, abandoned.

[30] **Foreign Application Priority Data**

Nov. 11, 1983 [JP] Japan 58-212083

[51] **Int. Cl.**[4] **G05F 3/24**

[52] **U.S. Cl.** **323/313**; 307/297; 307/304; 323/314; 323/349; 323/350; 365/226

[58] **Field of Search** ..... 323/311, 313, 349, 350, 323/314; 307/296 R, 297, 304; 365/226

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Primary Examiner—William H. Beha, Jr.

Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

A voltage converting circuit has an output MIS transistor which gives a low output impedance and outputs an intermediate level of power source voltage. The output level is set with a high accuracy through a voltage dividing ratio determined by an impedance element. This impedance element is connected with a compensating MIS transistor to compensate for variations of the gate threshold voltage caused by the manufacturing process.

10 Claims, 9 Drawing Figures

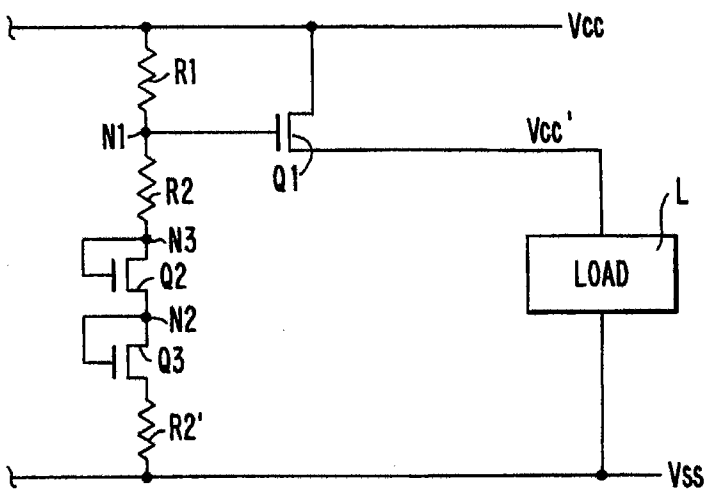


FIG. 1.
(PRIOR ART)

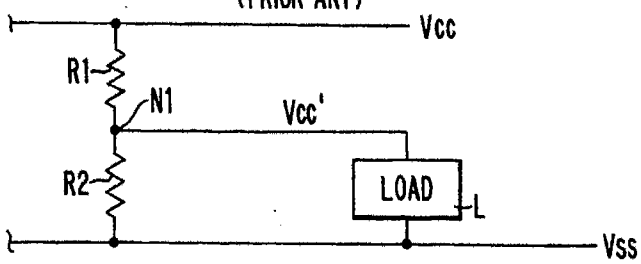


FIG. 2.
(PRIOR ART)

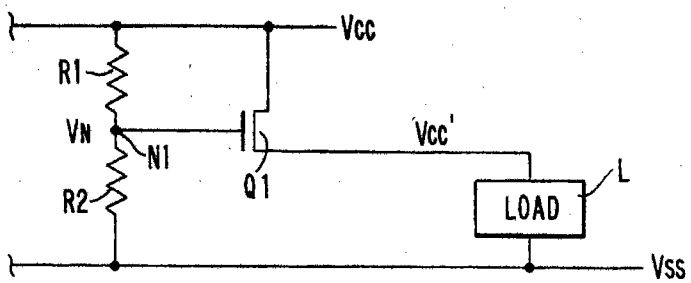


FIG. 8.

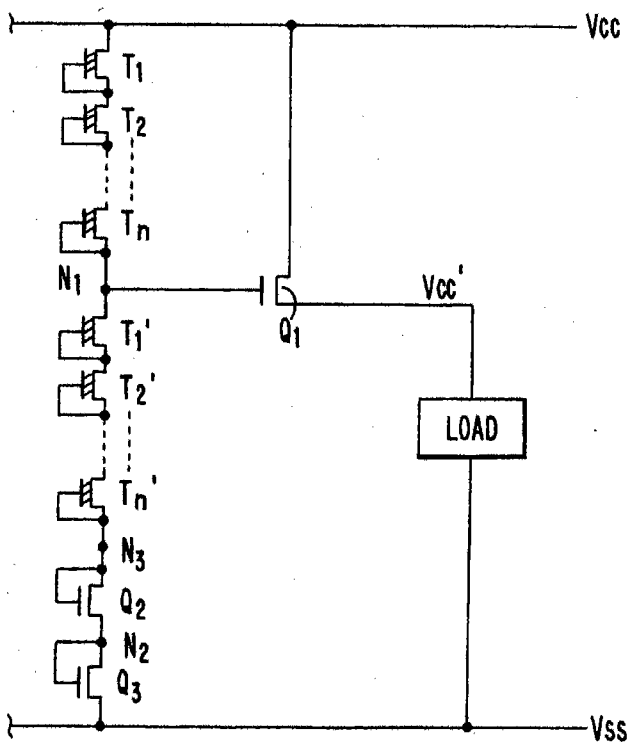


FIG. 3.

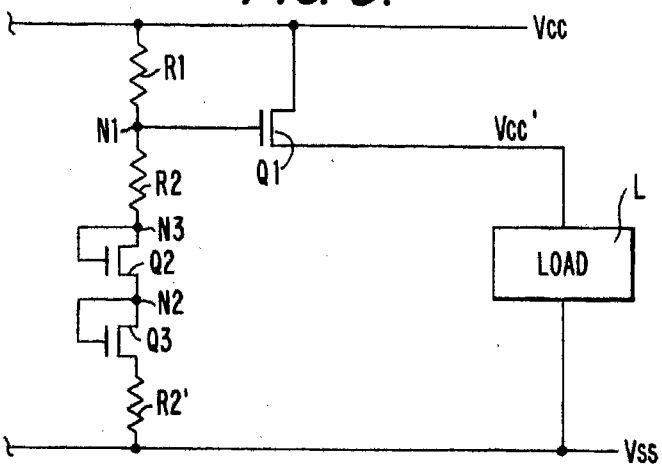


FIG. 4.

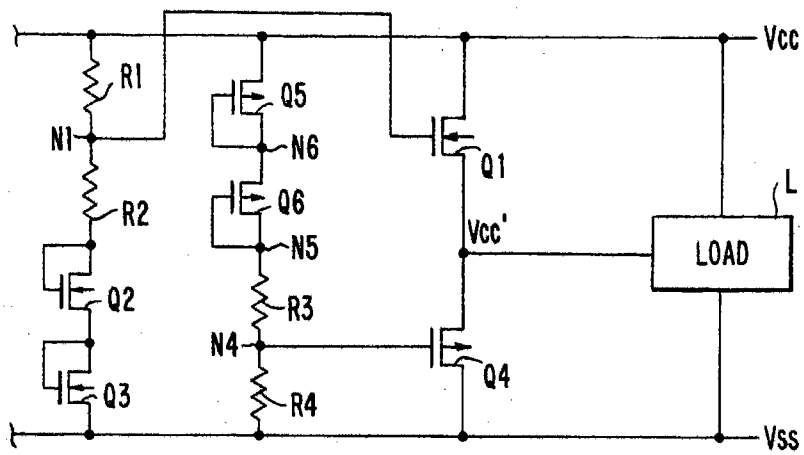


FIG. 5.

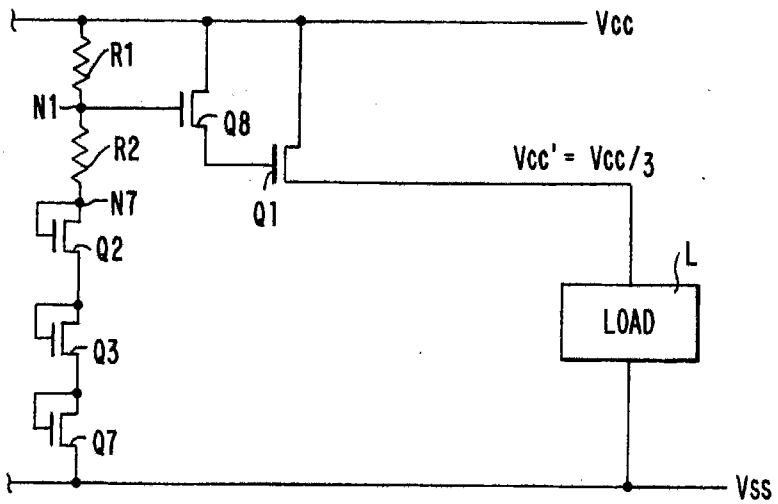


FIG. 6.

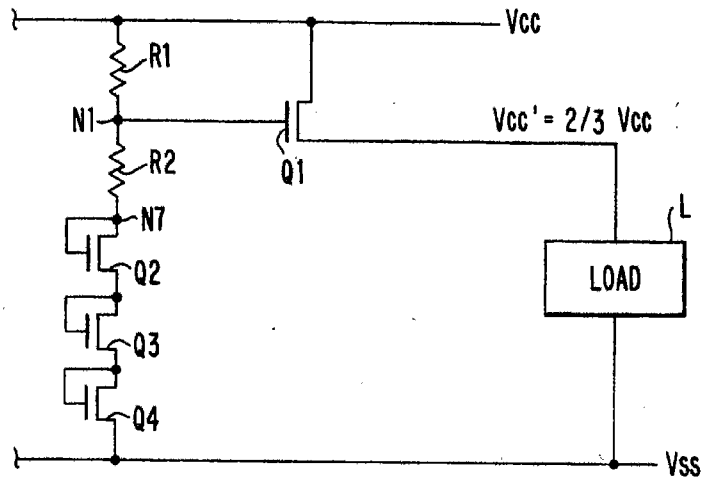


FIG. 7(a)

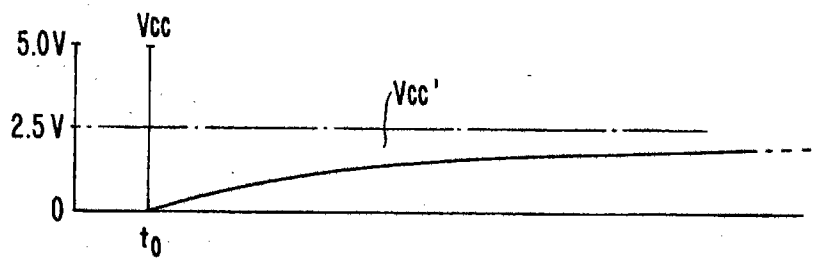
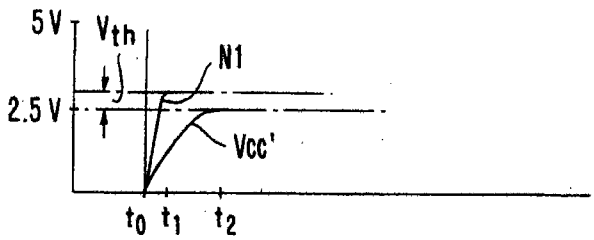


FIG. 7(b)



FET VOLTAGE REFERENCE CIRCUIT WITH THRESHOLD VOLTAGE COMPENSATION

This is a continuation of co-pending application Ser. No. 663,712 filed on Oct. 22, 1984, now abandoned 2/12/87.

BACKGROUND OF THE INVENTION

This invention relates to a voltage converting circuit which outputs an intermediate level of power supply voltage and particularly to a voltage converting circuit which is suitable for use in a MIS type integrated circuit.

It is often required in a MIS type integrated circuit to use a constant voltage having an intermediate level with respect to the power supply voltage supplied from an external circuit. For instance, an intermediate level of, for example, 2.5 V is steadily applied to a common capacitor electrode incorporated into memory cells in a MIS type dynamic random access memory operative under a power supply voltage of 5 V.

The intermediate level is obtained easily using a resistance dividing circuit as shown on FIG. 1. In this figure, resistors R_1, R_2 divide the power supply voltage V_{cc} in order to obtain an intermediate voltage V_{cc}' to be provided to a load circuit L. For a sufficiently low load current, when $R_1=R_2$, then $V_{cc}'=V_{cc}/2$. However, when a load circuit L consumes a current that is sufficiently high, such a relation is not maintained. Moreover, in this example, the resistors R_1, R_2 are connected in series between the power source V_{cc} of +5 V and the power source V_{ss} of 0 V, a current always flows from V_{cc} to V_{ss}, and thereby a large amount of power is consumed. This is one disadvantage of this circuit. Such power consumption can be reduced by making large the resistors R_1, R_2. However, if a resistance value is large, the above change in the voltage V_{cc}' at node N1 due to a load current becomes large.

The circuit shown in FIG. 2 is effective for reducing power consumption and fluctuation of the load voltage V_{cc}' due to a change of the load current. In this circuit, a divided voltage of power source V_{cc} obtained through the resistors R_1, R_2 is given to the gate of a MIS transistor Q_1 and an output of said transistor Q_1 is applied to the load circuit L. Q_1 constitutes an output transistor of low output impedance. Therefore, a load current flows through the drain and source of transistor Q_1 but does not flow into the voltage dividing circuit R_1, R_2. There is no change of load voltage V_{cc}' and, since the dividing circuit only gives a voltage to the gate of the MIS transistor Q_1, the circuit is allowed to have a high resistance value, thus resulting in less power consumption. Because of the relation $V_N-V_{th}=V_{cc}'$ between the voltage V_N of node N_1 and load voltage V_{cc}', when $V_{cc}'=V_{cc}/2$ is required, V_N is selected to have a value satisfying the relation, $V_N=V_{th}+V_{cc}/2$. V_{th} indicates the gate threshold voltage of the MIS transistor Q_1.

However, this circuit has a problem in that a threshold voltage V_{th} of the transistor Q_1 directly affects a load voltage V_{cc}' and V_{th} changes in accordance with the integration circuit manufacturing process, whereby the load voltage V_{cc}' fluctuates for each product.

Namely, it is well known that a resistance ratio of two resistors in an integrated circuit has only a small error, although there are changes of V_{th} depending on the manufacturing process. For example, it is easy to ensure that an error of resistance value ratio is as small as 1% or less. Therefore, a voltage V_N of node N_1 can be set accurately. Meanwhile, the gate threshold voltage of a MIS transistor is easily affected by a process fluctuation, and an error as small as 0.2 V can easily be generated. This error means, for example, that an error of about 10% easily occurs in the circuit for generating an output voltage V_{cc}' of 2.5 V.

SUMMARY OF THE INVENTION

An object of this invention is to provide a voltage converting circuit which outputs an intermediate level of power source voltage.

Another object of this invention is to provide a voltage converting circuit which consumes less power.

Yet another object of this invention is to provide a voltage converting circuit comprising an output MIS transistor which gives a small output impedance.

A further object of this invention is to prevent an output voltage from being affected by a variation of the threshold voltage V_{th} caused by a fluctuation in the manufacturing process for output MIS transistors of voltage converting circuits.

In accordance with the present invention, a voltage converting circuit is provided for receiving a power source voltage and providing a constant voltage having the level of a predetermined porportional division of said power source voltage, comprising:

an output MIS transistor for outputting said constant voltage, with the MIS transistor having a gate which receives a gate control voltage; and

a gate control means for providing said gate of said MIS transistor with said gate control voltage, comprising an impedance means connected to receive said power source voltage for providing said predetermined proportional division, and compensating means having at least one compensation MIS transistor connected to said impedance means, for compensating the gate control voltage for the gate threshold voltage of said output MIS transistor to provide said constant voltage corresponding to said predetermined proportional division irrespective of variation of said gate threshold voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and advantages of the present invention will be more apparent from the following description of the preferred embodiments with reference to the accompanying drawings, wherein:

FIG. 1 is a circuit diagram of a voltage converting circuit in the prior art;

FIG. 2 is a schematic diagram of the other voltage converting circuit in the prior art;

FIG. 3 is a schematic diagram of a voltage converting circuit in an embodiment of this invention;

FIG. 4 is a schematic diagram of a voltage converting circuit in another embodiment of this invention;

FIG. 5 is a schematic diagram of a voltage converting circuit in yet another embodiment of this invention;

FIG. 6 is a schematic diagram of a voltage converting circuit in a further embodiment of this invention;

FIGS. 7(*a*) and (*b*) are respective the graphs which show the change in time of the converted voltage output after the power source is turned ON in the circuits of the prior art and of the embodiments of this invention; and

FIG. 8 is a schematic diagram of a voltage converting circuit in still a further embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 3 shows an embodiment of this invention. From FIG. 1 to FIG. 8, the same portions as those in FIG. 1 and FIG. 2 are given the same symbols for convenience of description. In comparison with the circuit of the prior art as shown in FIG. 2, the circuit of FIG. 3 is different therefrom in such a point that the MIS transistors Q_2, Q_3 are inserted into the voltage dividing circuit (gate voltage control circuit). In the circuit of FIG. 3, a pair of N channel MIS transistors Q_2, Q_3 are connected in series to the resistor elements R_1 and R_2 which give a voltage dividing ratio. A divided output from the series circuit of resistor elements R_1, R_2 and MIS transistors Q_2, Q_3 is given at the node N_1 to the gate of the output N channel MIS transistor Q_1. The transistors Q_2, Q_3 are provided for compensating its gate threshold voltage, and the number of transistors depends on the voltage dividing ratio. The circuit of FIG. 3 is provided for outputting a voltage of $V_{cc}/2$ and two transistors Q_2 and Q_3 are required in this case. Said circuit of FIG. 3 operates normally when a voltage of the power source voltage supply line is higher than the normal voltage $V_{cc}/2$ to be output. In this case, the voltage of node N_2 is V_{th}, the voltage of node N_3 is $2\times V_{th}$. When $R_1=R_2$, the voltage of node N_1 is indicated by $(V_{cc}-2V_{th})/2+2V_{th}=V_{cc}/2+V_{th}$. Since the transistors Q_1, Q_3 are formed by the same process on a semiconductor substrate, these transistors can be considered to have the same threshold voltage. When the node N_1 has the above voltage, a load voltage V_{cc}' is $V_{cc}/2$, which is lower than the above voltage by V_{th}. Thereby, a voltage V_{cc}' irrespective of the threshold voltage of a transistor can be supplied to the load L.

FIG. 4 is a second embodiment of this invention. The circuit of FIG. 3 is based on the assumption that the load L always receives an input current through the transistor Q_1 (a current flows through V_{cc}-Q_1-L-V_{ss}) and that a current does not flow out from the load L toward the source of the transistor Q_1. However the circuit of FIG. 4 can operate properly even if current flows out from the load L. In this circuit, the circuit portion formed by R_1, R_2, Q_3, Q_2 is the same as that in FIG. 3, a load voltage V_{cc}' is held thereby to $V_{cc}/2$, irrespective of V_{th}. The MIS transistors Q_4, Q_5, Q_6 resistors R_3, R_4 form a circuit which holds the load voltage V_{cc}' to $V_{cc}/2$ in such a case where a current flows into the power supply V_{ss} through the transistor Q_4 from the load L. Here, Q_4, Q_5, Q_6 are P channel transistors. Namely, the voltage of node N_6 is $V_{cc}-V_{thp}$, the voltage of node N_5 is $V_{cc}-2V_{thp}$ and the voltage of node N_4 is $(V_{cc}-2V_{thp})/2=V_{cc}/2-V_{thp}$ when $R_3=R_4$. V_{thp} is the gate threshold voltage of the p channel transistor Q_4. Since a voltage of node N_4 is lower than V_{cc}' by V_{th} of Q_4, V_{cc}' becomes $V_{cc}/2$. In the circuit of FIG. 4, a load voltage can be set constant irrespective of a load voltage V_{th}, in either case where a current flows into the load or a current flows out from the load.

It is desirable in actual design of the circuit of FIG. 4 to assure the avoidance of a steady current in the series circuit of transistors Q_1 and Q_4 by providing a small difference between the voltage dividing ratio of the resistors R_1, R_2 and the voltage dividing ratio of the resistors R_3, R_4. For example, the voltage of node N_1 should advantageously be $V_{cc}/2+V_{th}$ minus several 10 mV and the voltage of node N_4 should be $V_{cc}/2-V_{thp}$ plus several 10 mV. Thereby, when the output voltage V_{cc}' is $V_{cc}/2$, both output transistors Q_1, Q_4 are set to the cut-off condition. IF the output voltage V_{cc}' rises or drops, the output transistors Q_1 or Q_4 become selectively ON and suppress the change of voltage described above.

FIG. 5 and FIG. 6 show the third and fourth embodiments of this invention. The former holds a load voltage V_{cc}' to $V_{cc}/3$, while the latter to $2V_{cc}/3$. Namely, since the voltage of node N_7 is $3V_{th}$ and the resistance values of resistors R_1, R_2 are selected in such a relation as $R_1=2R_2$ in FIG. 5, the voltage of node N_1 becomes equal to $(V_{cc}-3V_{th})/3+3V_{th}=V_{cc}/3+2V_{th}$, and the load voltage V_{cc}' is lower than this voltage level by $2V_{th}$ due to the voltage drop across transistors Q_8 and Q_1 thus becoming equal to $V_{cc}/3$. In FIG. 6, the voltage of node N_7 is $3V_{th}$, the voltage of node N_1 is $2(V_{cc}-3V_{th})/3+3V_{th}=2V_{cc}/3+V_{th}$ when $2R_1=R_2$, and the load voltage V_{cc}' is lower than this voltage by V_{th}, becoming equal to $2V_{cc}/3$.

In general, the load voltage of $V_{cc}'=mV_{cc}/n$ can be obtained by using n transistors as the transistors Q_2, Q_3, . . . to be inserted in series with the resistance voltage dividing circuit, of the gate voltage control circuit and $(n-m-1)$ transistors as the transistors Q_8 . . . to be inserted into the gate circuit of the output transistor Q_1, and by setting a resistance ratio $R_2/(R_1+R_2)$ to m/n. Thereby, a variety of load voltages V_{cc}' which are not affected by V_{th} can be obtained. In the above, m and n are integers for which $m<n$.

When the resistance value is made large in order to reduce power consumption in the resistance voltage dividing circuit, the time constant becomes large and the rising edge of the load voltage becomes gentle as shown in FIG. 7(*a*). In case a transistor Q_1 is used as in the case of FIG. 3, the load voltage V_{cc}' quickly rises as shown in FIG. 7(*b*) and, when the power supply becomes ON, operation can be started immediately.

In the circuit of FIG. 3, the resistor R_2 may be shifted, for example, to the location between Q_3 and V_{ss} from the location indicated. The alternate location for the resistor R_2 is indicated by the resistor R_2', shown with the dotted line in the lower left corner of FIG. 3. In this case, the same result can also be obtained. Moreover, this method is superior in such a point that each transistor Q_1, Q_2, or Q_3 receives a similar back gate bias effect on its own V_{th}, since the source voltage of Q_2, Q_3 rises up to a value close to that of Q_1 and, thereby, V_{th} of Q_2 and Q_3 becomes equal to that of Q_1.

FIG. 8 shows an embodiment where the resistors R_1, R_2 in FIG. 3 are replaced by depletion transistors T_1, T_n, T_1' T_n'. The same transistors and the same nodes are indicated by the same symbols. In general, a resistance of the polysilicon layer or diffusion layer used in a MIS dynamic memory is as small as several 10 ohms/square. If it is desired to obtain a resistance of several 100 k-ohm as required for the resistors R_1, R_2 by using these resistance layers, an area of several hundreds of thousand μ^2 becomes necessary. In order to avoid this, it is recommended to use one or a plurality of depletion transistors connected in series in place of resistors. Thereby, a current can be reduced using a small area.

I claim:

1. A voltage converting circuit for receiving a power source voltage and providing a constant voltage having a level of a predetermined proportional division of said power source voltage, comprising:

an output MIS transistor, having a gate and a threshold voltage, for outputting said constant voltage, wherein the gate of said output MIS transistor receives a gate control voltage; and

gate control means for providing said gate of said output MIS transistor with said gate control voltage, comprising

an output node for outputting said gate control voltage,

resistive means, including pairs of resistive elements connected in series via said output node and connected to receive said power source voltage, for determining said predetermined proportional division, each resistive element having a resistance being independent of said threshold voltage, and

compensating means, including a plurality of compensation MIS transistors connected in series with said resistive means, for compensating for the value of the threshold voltage of said output MIS transistor in the value of said gate control such that said constant voltage corresponding to said predetermined proportional division is output by said output MIS transistor irrespective of a common variation of the threshold voltage of each of said output and said compensation MIS transistors, the number of said compensation MIS transistors being in accordance with the proportion of said predetermined proportional division.

2. A voltage converting circuit as set forth in claim 1, wherein said resistive elements comprise a plurality of resistor elements connected in series with said compensation MIS transistors.

3. A voltage converting circuit as set forth in claim 1, wherein said resistive elements comprise a plurality of depletion MIS transistors connected in series with said compensation MIS transistors.

4. A voltage converting circuit as set forth in claim 1, wherein said output MIS transistor and each said compensation MIS transistor is produced in the same production process to have the same threshold voltage.

5. A voltage converting circuit as set forth in claim 1, wherein said impedance means comprises plural parts connected on opposite sides of said compensation MIS transistors.

6. A voltage converting circuit connected between first and second power source lines for supplying a power source voltage, for providing a constant voltage having an intermediate level with respect to said power source voltage, said circuit comprising:

first and second output MIS transistors respectively connected to said first and second power source lines and to each other to provide said constant voltage, the first and second output MIS transistor having respective first and second gates which receive first and second gate control voltages, respectively; and

first and second gate control means, for providing said first and second gates with said first and second gate control voltages respectively, comprising:

first and second impedance means each connected between said first and second power source lines for providing first and second proportional divisions of said power source voltage, respectively; and

first and second compensating means having first and second compensation MIS transistors connected to said first and second impedance means, respectively, for compensating the first and second gate control voltages for the respective gate threshold voltages of said first and second MIS transistors;

wherein said first and second output voltages are provided irrespective of variations of said gate threshold voltages, respectively.

7. A voltage converting circuit as set forth in claim 6, wherein each of said first output MIS transistor and said first compensation transistor comprises an N channel MIS transistor and each of said second output MIS transistors and said second compensation transistors comprises a P channel MIS transistor.

8. A voltage converting circuit as set forth in claim 6, wherein each said first and second impedance means has plural parts connected in series and on both sides of the respective first and second compensation MIS transistors.

9. A voltage coverting circuit as in claim 6, wherein at least one of said first and second output MIS transistors is in the cut-off state at any time.

10. A voltage converting circuit for receiving a power source voltage and providing a constant voltage having a level of a predetermined proporational division of said power source voltage defined by the ratio of m/n, wherein n and m are positive integers and m is less than n, comprising:

an output MIS transistor, having a gate and a threshold voltage, for outputting said constant voltage, wherein the gate of said output MIS transistor receives a gate control voltage; and

gate control means for providing the gate of said output MIS transistor with said gate control voltage, comprising

an output node for outputting said gate control voltage,

resistive means, including pairs of resistive elements connected in series via said output node and connected to receive said power source voltage, for determining said predetermined proportional division, each resistive element having a resistance being independent of said threshold voltage,

compensating means, connected in series with said resistive means, including first compensation MIS transistors, the number of said first compensation MIS transistors corresponding to the denominator n of said ratio of said predetermined proportional division,

at least a second compensation MIS transistor connected in parallel with a portion of said resistive means, for providing said gate control voltage to said gate of said output MIS transistor, the number of said second compensation MIS transistors corresponding to the numerator m of said ratio;

said gate control voltage having the level of said constant voltage plus a threshold voltage of said output MIS transistor.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 4,692,689
DATED : September 8, 1997
INVENTOR(S): TAKEMAE

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 1, col. 5, line 10,change "pairs" to --a pair--.

Claim 10, col. 6, line 42,change "pairs" to --a pair--.

Signed and Sealed this

Eighteenth Day of April, 2000

Attest:

Q. TODD DICKINSON

Attesting Officer *Director of Patents and Trademarks*

EXHIBIT K

United States Patent [19]

Matsui et al.

[11] **Patent Number: 4,527,070**

[45] **Date of Patent: Jul. 2, 1985**

[54] **METHOD AND APPARATUS FOR INSPECTING A PATTERN**

[75] Inventors: **Shougo Matsui**, Sagamihara; **Yoshimitu Mashima**, Kawasaki; **Kenichi Kobayashi**, Tokyo, all of Japan

[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[21] Appl. No.: **409,983**

[22] Filed: **Aug. 20, 1982**

[30] **Foreign Application Priority Data**

Aug. 20, 1981 [JP] Japan 56-131276

[51] **Int. Cl.**³ **G01N 21/86**

[52] **U.S. Cl.** **250/560**; 356/376

[58] **Field of Search** 364/468, 488–491; 250/556, 560; 358/101, 106; 356/400, 376

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Primary Examiner—David C. Nelms
Assistant Examiner—J. Jon Brophy
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

In a method for inspecting a pattern produced by using pattern data of a predetermined reference pattern, comparison is carried out between the pattern reproduced from the scanning signal of the pattern and the pattern produced from the signal of a modified form of the predetermined reference pattern.

12 Claims, 8 Drawing Figures

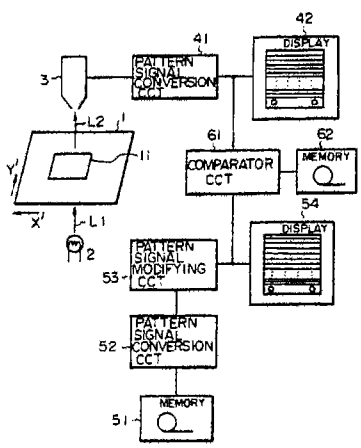
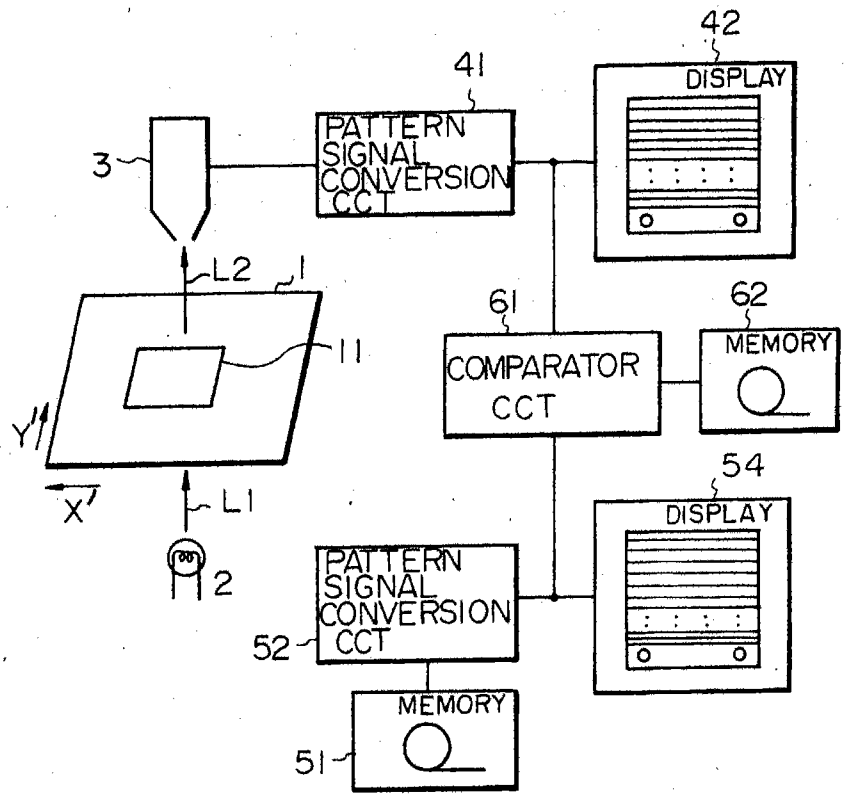


Fig. 1


42
41
DISPLAY
PATTERN SIGNAL CONVERSION CCT
3
L2
1
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61
62
COMPARATOR CCT
MEMORY
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54
DISPLAY
PATTERN SIGNAL CONVERSION CCT
52
MEMORY
51

Fig. 2

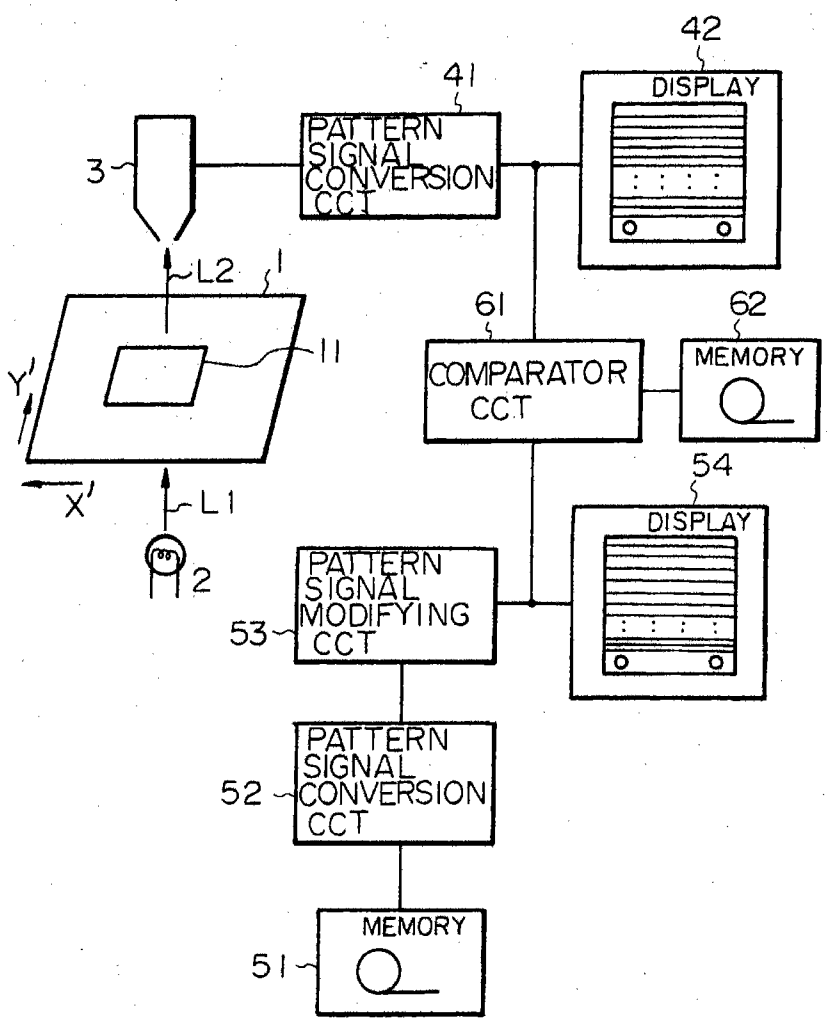

42
41
DISPLAY
PATTERN SIGNAL CONVERSION CCT
3
L2
1
61
62
11
COMPARATOR CCT
MEMORY
Y'
54
X'
L1
DISPLAY
2
PATTERN SIGNAL MODIFYING CCT
53
PATTERN SIGNAL CONVERSION CCT
52
MEMORY
51

Fig. 3

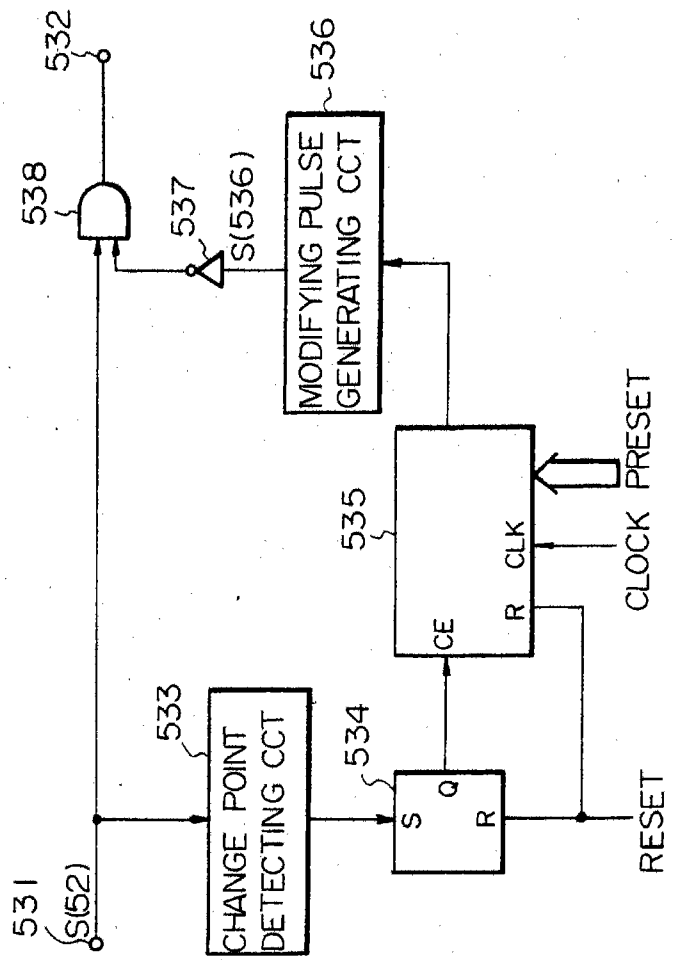

532
536
538
537
S(536)
MODIFYING PULSE GENERATING CCT
535
PRESET
CLK
CLOCK
R
CE
533
534
S
Q
R
CHANGE POINT DETECTING CCT
RESET
531
S(52)

Fig. 4

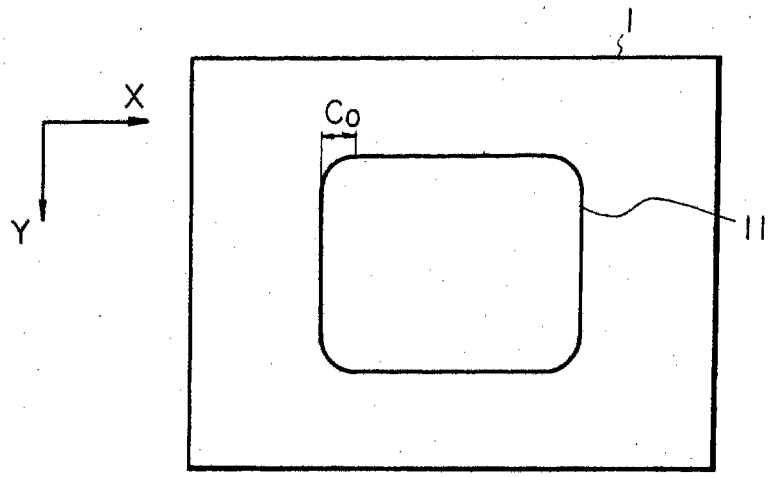


Fig. 5

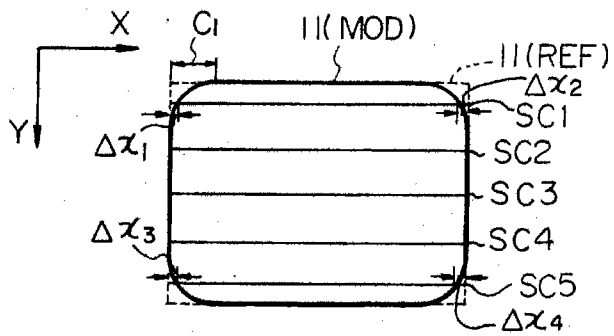


Fig. 6

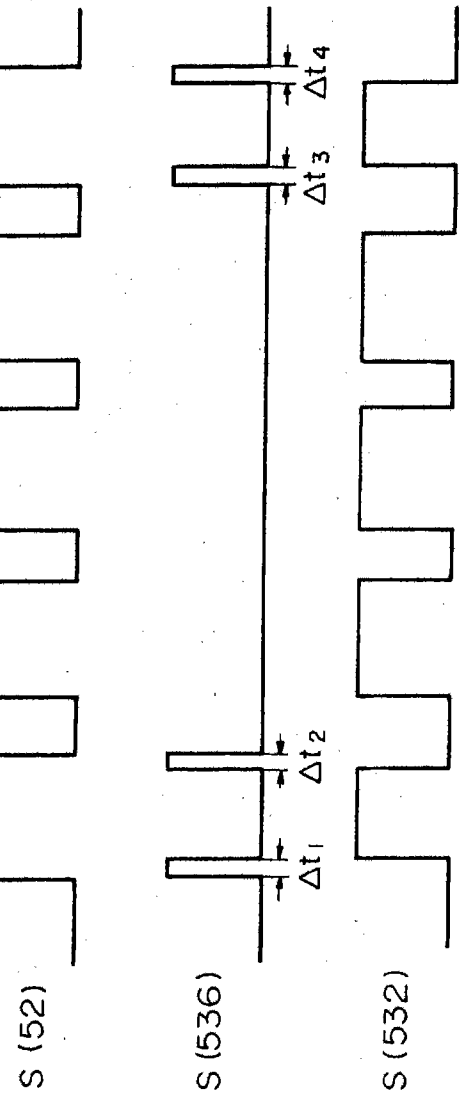


Fig. 7

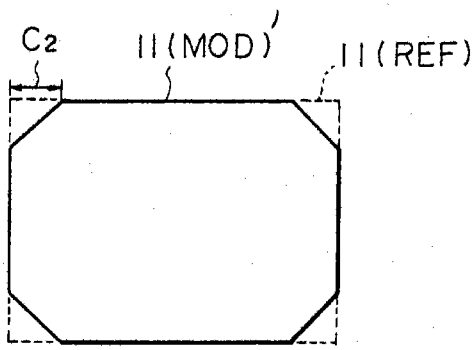
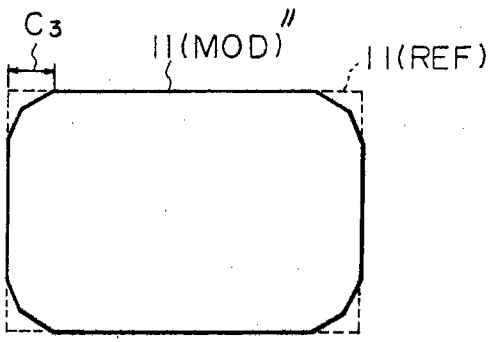


Fig. 8



METHOD AND APPARATUS FOR INSPECTING A PATTERN

BACKGROUND OF THE INVENTION

The present invention relates to a method and an apparatus for inspecting a pattern. The method of the present invention is used, for example, to inspect the pattern formed on a reticle used for producing master masks for producing semiconductor devices.

Photomasks used for producing semiconductor devices are produced by producing a pattern on a reticle approximately 10 times the size of the photomask, reducing the reticle to obtain a master mask, and copying the master mask. The reticle pattern is usually inspected using a microscope. However, such an inspection method requires a considerable number of steps. Further, the accuracy of the inspection is not satisfactory.

It is possible to inspect the reticle pattern using the apparatus illustrated in FIG. **1**, which will be introduced later in the brief description of the drawings. The apparatus of FIG. **1** comprises a glass plate **1** having a reticle pattern **11**, a light source **2** emitting a light beam L**1**, an image sensor **3** comprising, for example, a charge coupled device (CCD) receiving light beam L**2**, a pattern signal conversion circuit **41** for receiving the signal from the image sensor **3**, an actual pattern display device **42** comprising, for example, a TV monitor for receiving the signal from the pattern signal conversion circuit **41**, a memory device **51** comprising, for example, a magnetic tape, a pattern signal conversion circuit **52** for receiving the signal from the memory device **51**, a reference pattern display device **54** comprising, for example, a TV monitor for receiving the signal from the pattern signal conversion circuit **52**, a comparator circuit **61** for receiving the signals from the pattern signal conversion circuits **41** and **52**, and a memory device **62** comprising, for example, a magnetic tape for receiving the signal from the comparator circuit **61**.

In the device of FIG. **1**, the actual reticle pattern **11** on the plate **1** is scanned with the light beam L**1** emitted from the light source **2** by moving the glass plate **1** in the X′ direction from right to left, in the reverse-X′ direction from left to right, in the Y′ direction by a predetermined amount, in the X′ direction from right to left, and then in the reverse-X′ direction from left to right, and so on.

The pattern signal produced from the image sensor **3** is converted in the pattern signal conversion circuit **41** to output a signal to the actual pattern display device **42** and the comparator circuit **61**. The reference pattern signal is read out from magnetic tape **51** and supplied to the pattern signal conversion circuit **52** which outputs a signal to the reference pattern display device **54** and the comparator circuit **61**. The actual pattern and the reference pattern can therefore be visually compared and checked on the display devices **42** and **54**.

In the operation of the device of FIG. **1**, there exists the problem of missing the corners of the actual reticle pattern **11**. That is, the etching process using the photo resist layer as a mask and applied to the metal layer unavoidably causes loss of the corners of the actual reticle pattern. Hence, an actual reticle pattern with missing corner portions is obtained, as illustrated in FIG. **4**. The actual reticle pattern **11** of FIG. **4** has round corners. The length C_0 of one of the round corners in the X direction is, for example, less than approximately 1.2 microns. While actual patterns with missing

corners of more than 1.2 micron C_0 should be excluded as defective, actual patterns with the missing corners of less than 1.2 micron C_0 should be regarded as permissible even if they do not coincide exactly with the reference pattern.

However, since the reference pattern read out from the magnetic tape **51** is the precisely designed pattern, the reference pattern has no such round corners as in the actual pattern. Therefore, in the device of FIG. **1**, it is desired that the result of the comparison between the actual pattern and the reference pattern indicate the actual pattern to be defective only when the length C_0 of the round corner of the actual pattern exceeds a predetermined threshold length, such as 1.2 micron.

SUMMARY OF THE INVENTION

It is the principal object of the present invention to solve the above-described problem in the device of FIG. **1**, to provide an improved method for inspecting patterns by comparing the actual patterns and a reference pattern, to avoid unnecessary detection of allowable defective patterns, to carry out the detection only with respect to substantially defective patterns, and, accordingly, to reduce the cost of the production of patterns, such as reticle patterns.

According to the fundamental aspect of the present invention there is provided a method for inspecting a pattern which is produced by using pattern data of a predetermined reference pattern, comprising the steps of scanning the pattern to be inspected to produce a scanning signal of the pattern, reading out the pattern data of the predetermined reference pattern stored in a memory device, processing the read out pattern data of the predetermined reference pattern to provide a modified signal of the predetermined reference pattern, the modified signal corresponding to a permissible pattern which is formed by deleting corners from the reference pattern, and comparing the scanning signal of the pattern and the modified signal of the predetermined reference pattern.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an apparatus for inspecting a pattern according to a background art of the method and apparatus of the present invention;

FIG. **2** is an apparatus for inspecting a pattern according to an embodiment of the present invention;

FIG. **3** is an example of the structure of the pattern signal modifying circuit **53** of FIG. **2**;

FIG. **4** is an example of the pattern to be inspected;

FIG. **5** is an example of the modified reference pattern;

FIG. **6** is a waveform diagram of portions of the circuit of FIG. **3**; and

FIGS. **7** and **8** are other examples of the modified reference pattern.

DESCRIPTION OF THE PREFERRED EMBODIMENT

An apparatus for inspecting a pattern in accordance with an embodiment of the present invention is illustrated in FIG. **2**. In this embodiment, the pattern **11** is on a reticle **1** which is used for producing a photomask for producing semiconductor devices.

The apparatus of FIG. **2** comprises a glass plate **1** having a reticle pattern **11**, a light source **2** emitting a light beam L**1**, an image sensor **3** comprising, for exam-

ple, a charge coupled device (CCD) for receiving a light beam L2, a pattern signal conversion circuit **41** for receiving the signal from the image sensor **3**, an actual pattern display device **42** comprising, for example, a TV monitor for receiving the signal from the pattern signal conversion circuit **41**, a memory device **51** comprising, for example, a magnetic tape, a pattern signal conversion circuit **52** for receiving the signal from the memory device **51**, a pattern signal modifying circuit **53** for receiving the signal from the pattern signal conversion circuit **52**, and a reference pattern display device **54** comprising, for example, a TV monitor for receiving the signal from the pattern signal modifying circuit **53**.

The apparatus of FIG. **2** also comprises a comparator circuit **61** for receiving the signals from the pattern signal conversion circuit **41** and the pattern signal modifying circuit **53**, and a memory device **62** comprising, for example, a magnetic tape for receiving the signal from the comparator circuit **61**.

The pattern signal modifying circuit **53** carries out a modification of the reference pattern signal read out from the memory device **51** to produce a modified reference pattern with missing corners, that is, a modified reference pattern which is formed by deleting corners from the reference pattern.

An example of the structure of the pattern signal modifying circuit **53** is illustrated in FIG. **3**. The waveforms in the portions of the pattern signal modifying circuit **53** are illustrated in FIG. **6**. The pattern signal modification circuit **53** comprises an input line **531**, an output line **532**, a change point detecting circuit **533**, a set-reset circuit **534**, a counter circuit **535**, a modifying pulse generating circuit **536**, an inverter **537**, and an AND gate **538**.

The pattern **11** on the glass plate **1** is scanned by the light beam L1 emitted from the light source **2** beneath the glass plate **1**. The light beam L2 transmitted through the glass plate **1** is received by the image sensor **3** where the received light beam signal is transduced into an electrical signal. The output signal of the image sensor **3** is supplied to the pattern signal conversion circuit **41**. The output signal of the pattern signal conversion circuit **41** is supplied to the actual pattern display device **42** and one input of the comparator circuit **61**.

The modified reference pattern signal is produced by using the memory device **51**, pattern signal conversion circuit **52**, and pattern signal modifying circuit **53**. The process of the production of the modified reference pattern signal will be described with reference to FIG. **5** which illustrates the scanning lines SC1 through SC5 on the reference pattern **11** (REF), and FIG. **6** which illustrates the waveform of the scanning signal.

The reference pattern signal S(52) is supplied to input terminal **531** of a change point detecting circuit **533**. The change point detecting circuit **533** detects the point at which the indication of signal changes from white (light-transmitting) to black (light-interrupting), i.e., the point representing the edge of the pattern. The output signal of the change point detecting circuit **533** is supplied to the set-reset circuit **534**. The Q output of the set-reset circuit **534** is supplied to an input terminal (CE) of the counter **535**. In accordance with the output signal of the counter **535**, the modifying pulse generating circuit **536** produces the modifying pulse signal S(536) illustrated in FIG. **6**.

The width Δt, of the pulse S(536) is determined by the counter **535** which is controlled by the preset input signal PRESET.

The reference pattern **11** (REF) and the modified reference pattern **11** (MOD) are illustrated in FIG. **5**. The reference pattern **11** (REF) has a precise rectangular shape. The modified reference pattern **11** (MOD), which is drawn in a solid line, has round corners. The length C_1 of the round corner corresponds to the length C_0 of the round corner of the actual pattern illustrated in FIG. **4**.

Comparing FIG. **5** and FIG. **6**, it will be understood that the width Δt_1 corresponds to the length Δx_1 along the scanning line SC1.

The output signal S(536) of the modifying pulse generating circuit **536** is supplied to the inverter **537**. The output signal of the inverter **537** is supplied to one input of the AND gate **538**. The other input of the AND gate **538** receives the signal S(52). Thus, the production of the output signal of the AND gate **538** is inhibited during the occurrence of the signal S(536), so that the signal S(532) is produced as illustrated in FIG. **6**. The width Δt_2 in the pulse S(536) corresponds to the length Δx_2 along the scanning line SC1. The widths Δt_3 and Δt_4 in the pulse S(536) correspond to the lengths Δx_3 and Δx_4 along the scanning line SC5.

As described above, the modified reference pattern **11** (MOD) is obtained from the reference pattern **11** (REF). The signal representing the thus obtained modified pattern **11** (MOD) is supplied from the pattern signal modification circuit **53** to the other input of the comparator circuit **61** and to the reference pattern display device **54**.

Accordingly, the comparison between the actual pattern and the modified reference pattern is carried out in the comparator circuit **61**. The comparator circuit **61** produces the output signal indicating the occurrence of inconsistency when the difference between the signal of the actual pattern and the signal of the modified reference pattern exceeds a predetermined threshold value.

Also, a visual comparison can be made by viewing patterns displayed on the actual pattern display device **42** and the reference pattern display device **54**. Thus, unnecessary detection of the difference in the corners between the actual pattern **11** on the reticle **1** and the reference pattern stored in the memory device **51** is avoided.

In the device of FIG. **2**, the output signal of the comparator circuit **61** is stored in the memory device **62** comprising, for example, a magnetic tape. When the comparison of one pattern is completed, the set-reset circuit **534** and the counter **63** are reset by the reset signal RESET (FIG. **3**).

Although the preferred embodiment has been described heretofore with reference to FIGS. **2** through **6**, it will be understood that various modifications or alterations are possible without departing from the scope of the present invention. For example, instead of the modified reference pattern of FIG. **5**, other modified reference patterns of FIG. **7** and FIG. **8** can be used. The modified reference pattern **11** (MOD)' of FIG. **7** has corners formed by a single straight line cut. The modified reference pattern **11** (MOD)'' of FIG. **8** has corners formed by a bent straight line cut. The lengths C_2 and C_3 of the corner cut portions of FIGS. **7** and **8** are, for example, approximately 0.5 micron through 2.5 micron.

We claim:

1. A method for inspecting a pattern which is produced by using pattern data for a predetermined reference pattern having corners and being stored in a memory device, comprising the steps of:

(a) scanning the pattern to be inspected to produce a scanning signal;

(b) reading out the pattern data of the predetermined reference pattern stored in the memory device;

(c) processing the pattern data of the predetermined reference pattern to provide a modified form signal corresponding to a permissible pattern which is formed by deleting corners from the predetermined reference pattern; and

(d) comparing the scanning signal of the pattern and the modified form signal of the predetermined reference pattern.

2. A method as defined in claim 1, wherein said scanning step (a) comprises scanning a reticle pattern used for producing master masks for semiconductor devices.

3. An apparatus for inspecting a pattern which is produced by using pattern data of a predetermined reference pattern having corners, comprising:

scanning means for scanning the pattern to be inspected, said scanning means including:

a light source generating a light beam;

an image sensor operatively connected to sense said light beam and generate signals;

a stage for supporting the pattern; and

driving means, operatively connected to said stage, for driving said stage;

pattern signal conversion means, operatively connected to said image sensor, for receiving the signals from said image sensor and generating a scanning signal;

memory means, operatively connected to said pattern signal conversion means, for storing the pattern data of the predetermined reference pattern and providing a signal;

reference pattern signal conversion means, operatively connected to said memory means, for receiving said signal from said memory means and generating a pattern signal of the predetermined reference pattern;

signal modifying means, operatively connected to said reference pattern signal conversion means, for modifying the pattern signal of the predetermined reference pattern and generating a modified signal of the predetermined reference pattern, the modified signal corresponding to a permissible pattern which is formed by deleting the corners from the predetermined reference pattern; and

comparator means, operatively connected to said pattern signal conversion means and said signal modifying means, for comparing the scanning signal from said pattern signal conversion means and the modified signal of the predetermined reference pattern from said signal modifying means.

4. An apparatus, operatively connected to a memory for storing predetermined reference pattern data, the pattern being produced from pattern data of a predetermined reference pattern, the predetermined reference pattern having corners, for inspecting a pattern supported by a stage, comprising:

scanning means for scanning the pattern and outputting a scanning signal corresponding to the pattern;

a pattern signal conversion circuit, operatively connected to said scanning means, for receiving the scanning signal and generating a pattern signal;

a reference pattern signal conversion circuit, operatively connected to the memory, for receiving the predetermined reference pattern data and outputting a converted signal; a pattern signal modifying circuit, operatively connected to the reference pattern signal conversion circuit, for modifying the pattern signal of the predetermined reference pattern and generating a modified pattern signal, accordingly, the modified pattern signal corresponding to a permissible pattern which is formed by deleting the corners from the predetermined reference pattern;

a comparator, operatively connected to said pattern signal modifying circuit and said pattern signal conversion circuit, for receiving the modified pattern signal and the pattern signal and outputting a signal corresponding to the difference between the modified pattern signal and the pattern signal; and

first and second pattern display devices, operatively connected to said reference pattern signal conversion circuit and said pattern signal modifying circuit, for receiving and displaying the modified pattern signal and the pattern signal, respectively.

5. An apparatus as defined in claim 4, wherein said pattern signal modifying circuit comprises:

a change point detecting circuit, operatively connected to the reference pattern signal conversion circuit, for receiving the converted signal, detecting the edge of the pattern and outputting a first signal;

a set/reset circuit, operatively connected to said change point detecting circuit, for receiving the first signal and outputting a second signal;

a counter, operatively connected to said set/reset circuit, for receiving the second signal and outputting a third signal;

a modifying pulse generating circuit, operatively connected to said counter, for generating a modified pulse signal in accordance with the third signal;

an inverter, operatively connected to said modifying pulse generating circuit, for receiving the modified pulse signal and outputting an inverted modified pulse signal; and

an AND gate, operatively connected to said inverter and said reference pattern signal conversion circuit, for receiving the inverted modified pulse signal and the converted signal and producing the modified reference pattern signal in dependence upon the modified pulse signal.

6. An apparatus as defined in claim 4, wherein said modified pattern signal is generated when the corners of the predetermined reference pattern are cut by a single straight line.

7. An apparatus as defined in claim 4, wherein said modified pattern signal is generated when the corners of the predetermined reference pattern are cut by two straight lines at an angle to each other.

8. An apparatus as defined in claim 4, wherein said modified pattern signal is generated when the corners of the predetermined reference pattern are substantially rounded.

9. A method for inspecting a pattern produced by using pattern data corresponding to a predetermined reference pattern having corners and stored in a memory device, comprising the steps of:

(a) scanning the pattern to be inspected to produce a scanning signal;

(b) reading out pattern data corresponding to the predetermined reference pattern stored in the memory device;

(c) modifying the pattern data of the predetermined reference pattern to provide a modified form signal corresponding to a permissible pattern, by the substeps of:

(i) applying the pattern signal to a change point detecting circuit for detecting the edge of the pattern and outputting a first signal;

(ii) supplying the first output signal to a counter which outputs a second signal;

(iii) producing a modified form signal in accordance with the second output signal of the counter;

(d) comparing the scanning signal and the modified form signal to determine whether the pattern inspected is a correct pattern.

10. A method as defined as claim **9**, wherein said step (iii) comprises producing a modified form signal corresponding to when the corners of the pattern are cut by a single straight line.

11. A method as defined in claim **9**, wherein said substep (iii) comprises producing a modified form signal corresponding to when the corners of the pattern are cut by two straight lines at an angle to each other.

12. A method as defined in claim **9**, wherein said substep (iii) comprises producing a modified form signal corresponding to when the corners of the pattern are substantially rounded.

* * * * *

EXHIBIT L

United States Patent [19]

Abe

[11] **4,384,918**

[45] **May 24, 1983**

[54] **METHOD AND APPARATUS FOR DRY ETCHING AND ELECTROSTATIC CHUCKING DEVICE USED THEREIN**

[75] Inventor: **Naomichi Abe**, Tokyo, Japan

[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[21] Appl. No.: **304,902**

[22] Filed: **Sep. 23, 1981**

[30] **Foreign Application Priority Data**

Sep. 30, 1980 [JP] Japan 55-136255
Oct. 8, 1980 [JP] Japan 55-141046

[51] **Int. Cl.**³ **C23C 15/00**

[52] **U.S. Cl.** ..... **156/643**; 156/345; 204/192 E; 204/298; 361/234

[58] **Field of Search** ..... 156/345, 643; 204/192 E, 298; 279/1 R, 1 M; 271/18.1, 18.2, 193; 198/691; 361/234; 118/500

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Primary Examiner—Jerome W. Massie
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

An electrostatic chucking device is positioned on a supporting base, the temperature of which is maintained at a predetermined value, the device having an insulator, and a pair of plane electrodes on the insulator, and a material being chucked on the bottom surface of the top surface of the insulator, wherein the sum of the area of portions of the pair of plane electrodes facing the direction of the material being approximately equal to the contact area between the material and the insulator, and wherein a voltage is applied between the plane electrodes from an external power source, thereby effectively electrostatically chucking the material to the supporting base. A method and an apparatus for dry etching of a material having at least a conductive portion therein, the material being chucked by using said electrostatic chucking device mounted on a supporting base, the temperature of which is maintained at a predetermined value, in at least one of a sputter etching apparatus, a reactive sputter etching apparatus, or a plasma etching apparatus, whereby the material is indirectly chucked to the supporting base, the heat conductivity between the material and the supporting base is increased, the temperature of the material is controlled effectively, and the material can be held invertedly in the horizontal plane or vertically.

18 Claims, 10 Drawing Figures

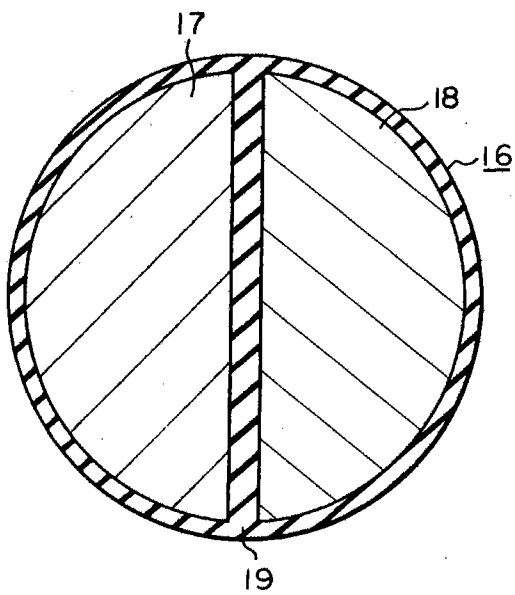

Fig. 1
(PRIOR ART)

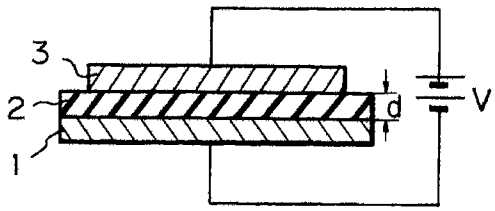

Fig. 2
(PRIOR ART)

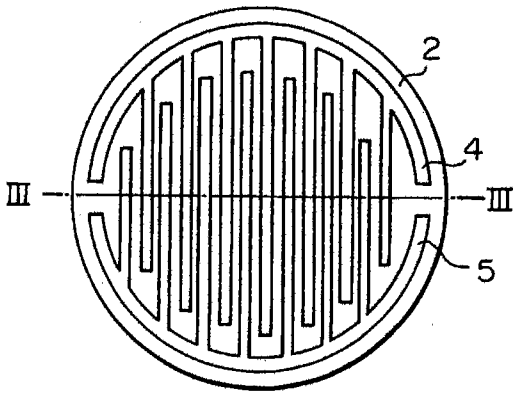

Fig. 3
(PRIOR ART)

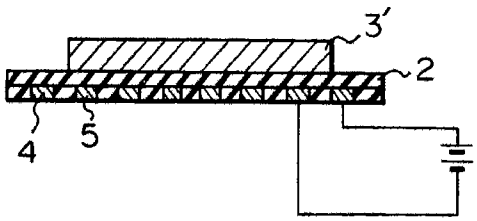

Fig. 4

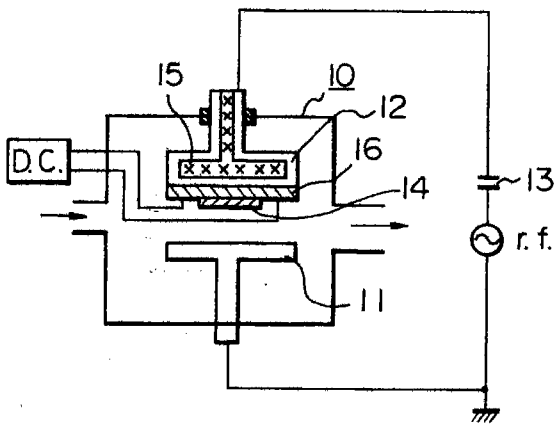

Fig. 5

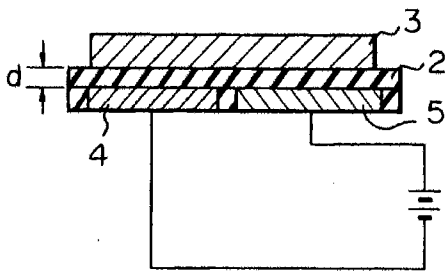

Fig. 6

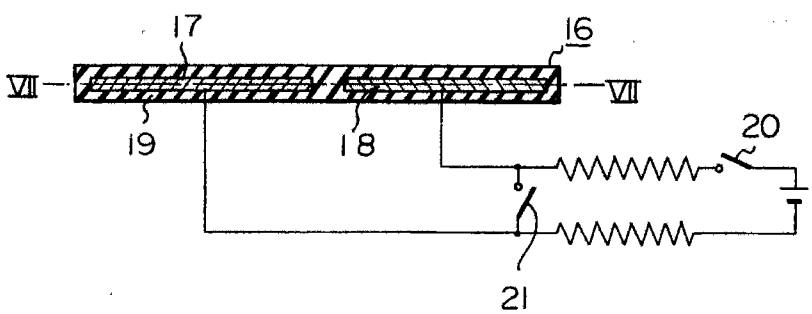

Fig. 7

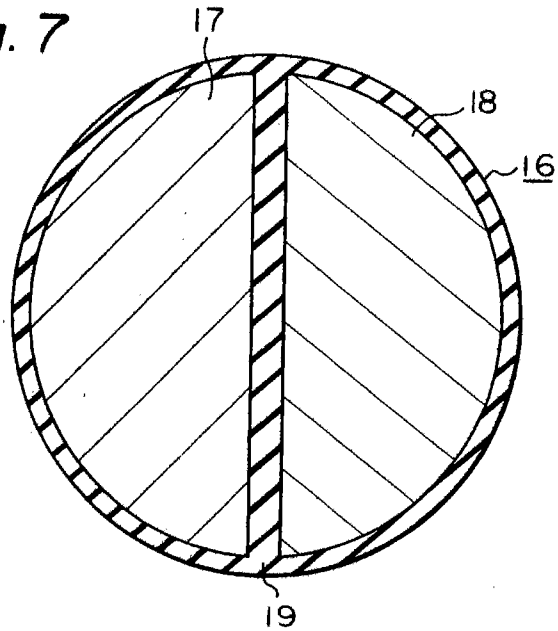

Fig. 8

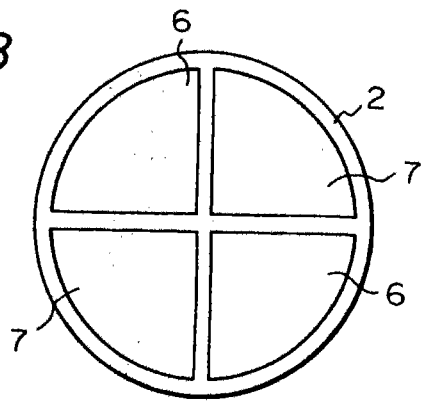

Fig. 9

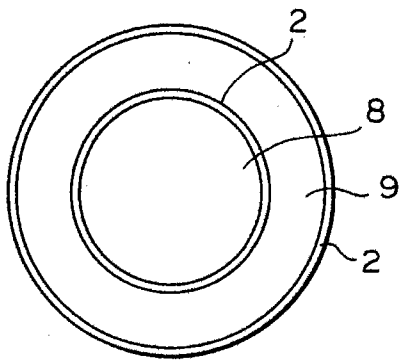

Fig. 10